

January 1996

CMOS LSI

SPECTRUM SPREAD CLOCK GENERATOR

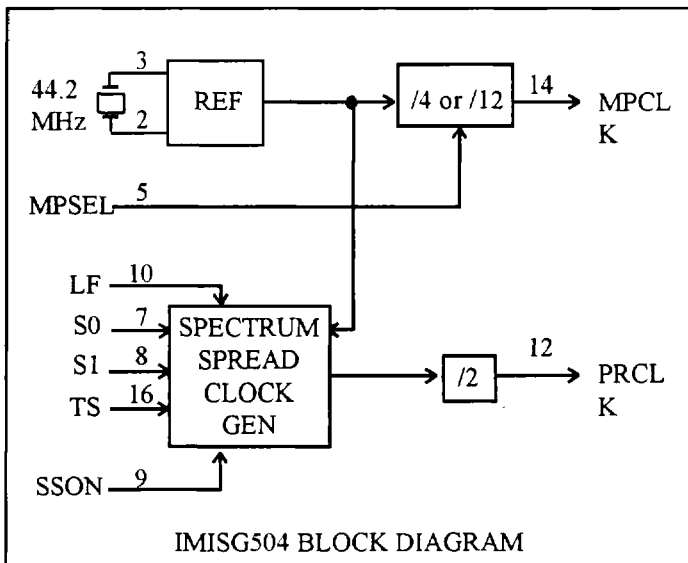
## PRODUCT FEATURES

- Generates CPU Clock Signals for Microprocessor Systems
- Reduces Measured EMI by 10 dB Nominal
- 4V to 7V Operating Supply Range
- supports 80286-, 80386-, 80486-, Pentium™ and 29000-Based Designs
- Wide Range of Selectable Output Frequencies Including 50, 60, 100 and 120 Mhz
- Single, Low Cost Crystal Used as Reference Frequency
- Glitch-Free Switching
- Power Down Mode for Low Power Consumption
- TTL or CMOS Compatible Outputs with 6 mA Drive Capability
- Pin Compatible with IMISC501 and IMISG502
- 16 PDIP and 16 PIN SOIC (300 Mil Body) Package Options

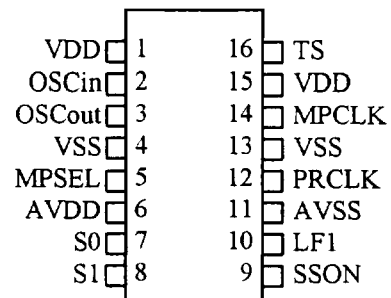
## PRODUCT DESCRIPTION

The IMISG504 is a spectrum spread clock generator specially designed for personal computers, laser printers and other digital systems. IMISG504 uses a patent pending concept to generate popular clock frequencies that are intentionally broadbanded to reduce electromagnetic interference. IMISG504 attenuates the radiated emission amplitudes from products associated with either the clock harmonics or any signals derived from the clock signals nominally 10 dB and could significantly reduce the cost of complying with the regulatory requirements.

PRCLK is the broadbanded output and can be programmed to generate 50, 60, 100 and 120 Mhz with the S0 and S1 pins. A single, low cost external crystal is required as reference frequency for the synthesizer. Output modulation function can be turned off with the SSON pin. Power down mode adds the flexibility to operate the device in a completely static mode to reduce standby currents and simplify system board tests. PRCLK output is modulated 3.75%.



## P-DIP/SOIC CONNECTION DIAGRAM



## APPLICATIONS

IMISG504 eliminates the need for multiple oscillators and generates the CPU clock signals for personal computers, laser printers and other digital systems. Supports 8086-, 80286-, 80386-, 80486-, Pentium™- and 29000-based designs. IMISG504 can be used with laptop or notebook computers to save power by running the system slower than normal CPU speeds or completely disabling the clocks in standby mode.

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## PIN DESCRIPTION

**OSCI<sub>n</sub>, OSC<sub>o</sub><sub>ut</sub>** - These pins form an on-chip reference oscillator when connected to terminals of an external 44.2 Mhz third overtone parallel resonant crystal. OSC<sub>in</sub> may also serve as an input for an externally generated CMOS level or AC coupled reference signal.

**S<sub>0</sub>, and S<sub>1</sub>** - Frequency select inputs. These inputs control the PRCLK frequency selection. S<sub>0</sub>-S<sub>1</sub> inputs control the CPU clock frequencies. All these inputs have internal pull-downs.

**PRCLK** - Output from the spectrum spread clock generator. Frequency selection is shown in Table 1.

Table 1 shows the output frequency selection conditions.

**TS** - Controls power down and Tri-State Mode selection. When high, S<sub>1</sub> input controls the mode selection as shown in Table 1 and Table 2. When low, device operates in normal mode. This pin has an internal pull-down.

**LF1** - This is the control output for the clock generator, It is a single-ended, tri-state output. Component connections are shown in Figure 1.

**SSON** - This pin controls the spectrum spread function. When low, PRCLK is modulated. When high, spreading is turned off. This pin has an internal pull-up.

**MPSEL** - Controls MPCLK output frequency selections. Table 2 shows the selected frequencies for MPCLK. This input has an internal pull-up.

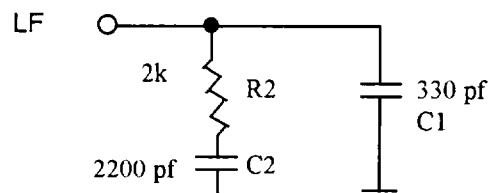
**MPCLK** - This is a nonmodulated output. This output can be programmed to be 3.7 Mhz or 11.06 Mhz. The selection of these frequencies are controlled by the MPSEL pin shown in Table 1.

**VSS** - Circuit ground.

**VDD** - Positive power supply.

**AVSS** - Analog circuit ground.

**AVDD** - Analog positive power supply.



**PRCLK FREQUENCY TABLE**

INPUTS			OUTPUT
TS	S1	S0	PRCLK
0	0	0	50 MHz
0	0	1	100 MHz
0	1	0	60 MHz
0	1	1	120 MHz
1	0	0	0; Power Down
1	0	1	1; Power Down
1	1	0	TEST
1	1	1	Hi-Z

**TABLE 1:** When Power Down address is selected, the VCO is turned off and the device goes to standby mode. Phase detector is in tri-state mode. The Table is based on using 44.2 Mhz crystal. Output can be scaled down using lower frequency crystals, see page 6.

**MPCLK FREQUENCY SELECTION**

INPUTS				OUTPUT
TS	MPSEL	S1	S0	MPCLK
0	0	X	X	3.7 Mhz
0	1	X	X	11.06 MHz
1	X	0	0	0; Power Down
1	X	0	1	1; Power Down
1	X	1	0	TEST
1	X	1	1	Hi-Z

**TABLE 2:** When Power down address is selected, the VCO is turned off and the device goes to standby mode. Phase detector is in tri-state mode.

# IMISG504

# SYSTEM CLOCK CHIP

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## MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VD:	0.3V
Storage Temperature	-65°C to 150°C
Ambient Temperature:	0°C to 70°C
Recommended Operating Range:	4.5 - 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

All inputs are tied high or low internally.

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Input Low Voltage	$V_{IL}$	-	-	0.8	Vdc
Input High Voltage	$V_{IH}$	2.0	-	-	Vdc
Input Low Current with Pull-up or Pull-down	$I_{IL}$	-	-	10/100	$\mu A$
Output Low Voltage $I_{OL} = 6mA$	$V_{OL}$	-	-	0.4	Vdc
Output High Voltage $I_{OH} = 6mA$	$V_{OH}$	2.5	-	-	Vdc
Tri-State leakage Current	$I_{OZ}$	-	-	10	$\mu A$
Static Supply Current	$I_{DD}$	-	-	250	$\mu A$
Dynamic Supply Current	$I_{CC}$	-	25	30	mA
Short Circuit Current	$I_{SC}$	25	-	-	mA

$V_{DD} = 5V \pm 10\%$ ,  $T_A = 0^\circ C \text{ to } 70^\circ C$

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## SPECTRUM SPREAD CLOCK. MODULATION SELECTION TABLE

	Bandwidth Limit Frequencies as a % Value of PRCLK	
	Low	High
Clock Spread	96.25%	100%

## SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Output Rise and Fall Time Measured at 10% - 90% of VDD	$t_{TLH}, t_{THL}$	-	-	5	ns
Output Rise and Fall Time Measured at 0.8V - 2.0V	$t_{TLH}, t_{THL}$	-	-	TBD	ns
Output Duty Cycles	$T_{sym}F1$	-	-	45/55	%
Jitter One Sigma	$tj1s$	-	-	2	% of Fout

$VDD = 5V \pm 10\%$ ,  $TA = 0^{\circ}C$ ,  $CL = 15pF$

## OSCILLATOR CHARACTERISTICS

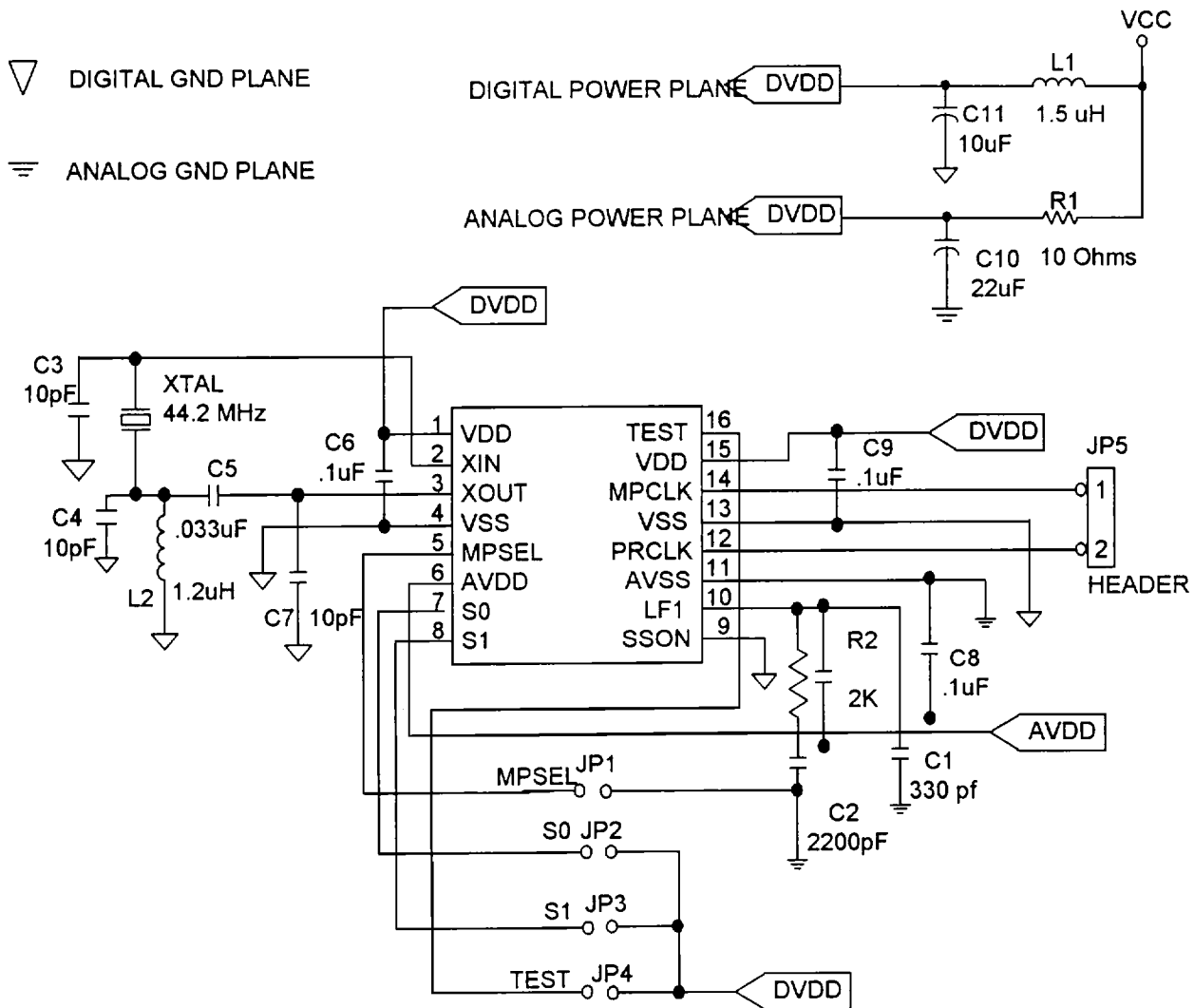
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Transconductance	gm	20	80	180	millimhos	@44.2 Mhz
Output Impedance	$Z_o$	-	200	800	ohms	@ 44.2 Mhz
Input Capacitance	$C_i$	8	13	18	pf	-
Output Capacitance	$C_o$	3	6	9	pf	-
DC Bias Voltage	$V_B$	1.5	VDD/2	3.5	Volt	-
Start-up Time	ts	-	-	2	ms	@ VDD = 4.5V

$VDD = +3.1V$  to  $+5.5V$ ,  $TA = 0^{\circ}C$  to  $70^{\circ}C$

## VCO CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
VCO Gain	$K_0$	35	55	65	Mhz/volt	$\Delta F/\Delta V$ Measured with VCO Control at 2V - 3V
Phase Detector Gain	$K_d$	100	145	200	$\mu A$	-

## EXTERNAL CONNECTIONS



NOTE1: KEEP C3, C4, C5, C6 CLOSE TO THEIR PINS (4, 11, 13, 10, 9 RESPECTIVELY).

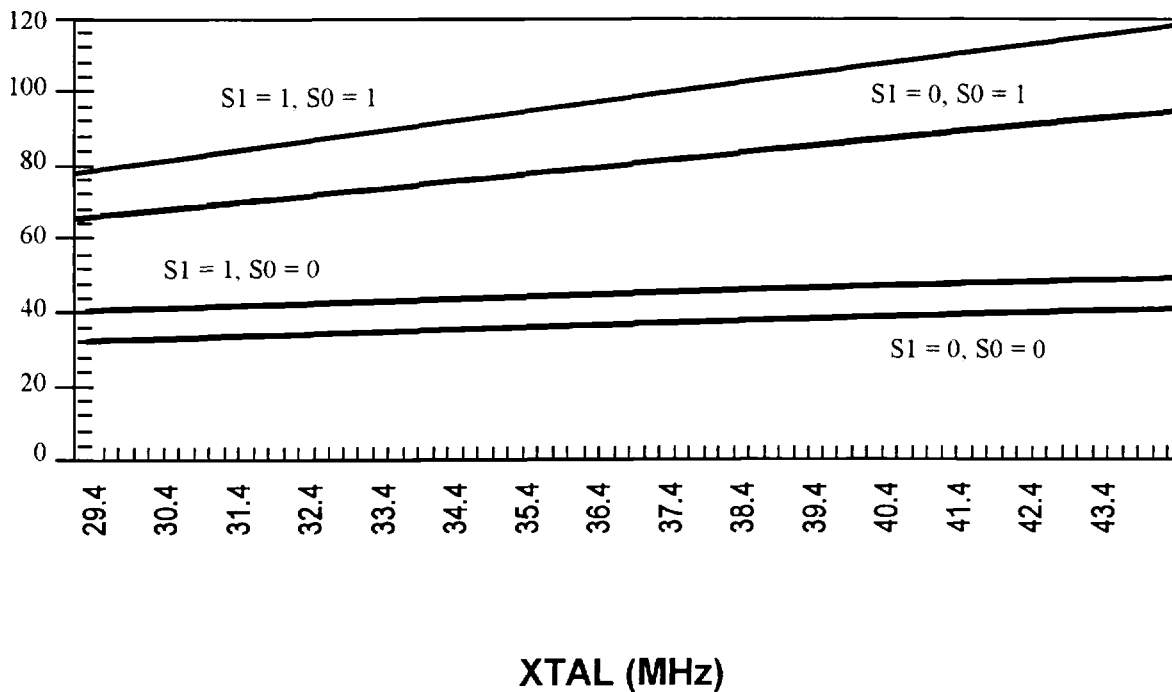
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## REFERENCE FREQUENCY VS OUTPUT FREQUENCIES

### PRCLK VS XTAL



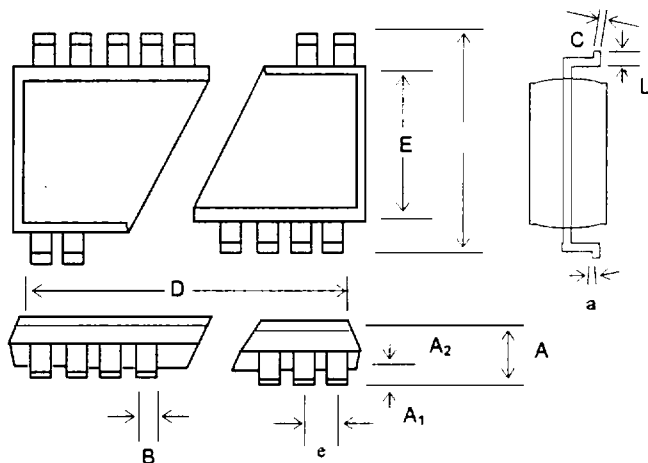
# IMISG504

# SYSTEM CLOCK CHIP

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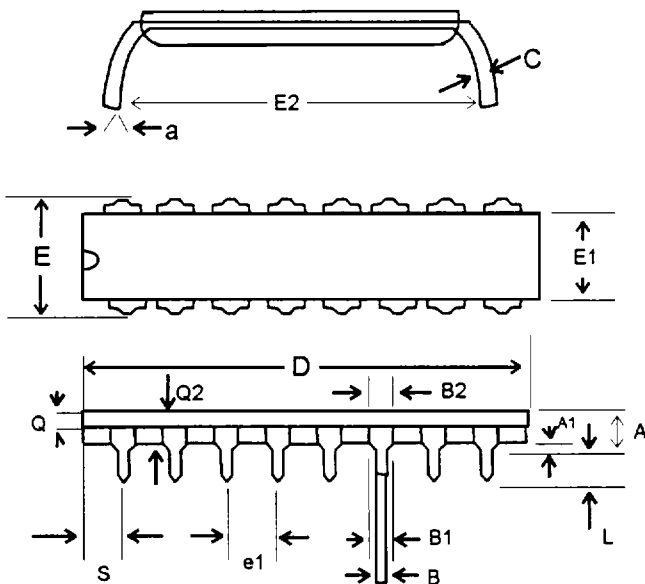
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## PACKAGE DRAWING AND DIMENSIONS



### 16 PIN SOIC OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A <sub>1</sub>	0.002	0.005	0.008	0.05	0.13	0.21
A <sub>2</sub>	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.06	0.009	0.13	0.15	0.22
D	0.239	0.244	0.249	6.07	6.20	6.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95



### 16-PIN PLASTIC DIP DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.150	0.160	0.170	3.81	4.06	4.318
A <sub>1</sub>	0.015	-	-	0.381	-	-
B	0.016	0.018	0.020	0.40	0.45	0.50
B <sub>1</sub>	0.056	0.059	0.062	1.47	1.52	1.57
B <sub>2</sub>	0.046	0.049	0.052	1.17	1.24	1.32
C	0.008	0.010	0.012	0.20	0.25	0.30
D	0.748	0.750	0.752	19.00	19.05	19.10
E	0.300	0.312	0.325	7.62	7.924	8.255
E <sub>1</sub>	0.240	0.252	0.260	6.096	6.49	6.604
E <sub>2</sub>	0.335	0.345	0.355	8.51	8.76	9.01
e <sub>1</sub>	0.100 BSC			2.54 BSC		
L	0.25	0.230	0.135	3.175	3.30	3.429
a	0°	7°	15°	0°	7°	15°
Q <sub>1</sub>	0.059	0.060	0.061	1.50	1.53	1.55
Q <sub>2</sub>	0.128	0.130	0.132	3.25	3.30	3.35
S	0.073	0.075	0.077	1.85	1.90	1.95

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## ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG504xPB	16 Pin Plastic Dip	Commercial, 0°C to + 70°C
IMISG504xB	16 Pin SOIC	Commercial, 0°C to +70°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI  
SG504xPB  
Date Code, Lot #

