SOT-23 Formed SMD Package **CSC2712**

SILICON PLANAR EPITAXIAL TRANSISTOR

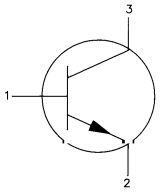
N-P-N transistor

Marking

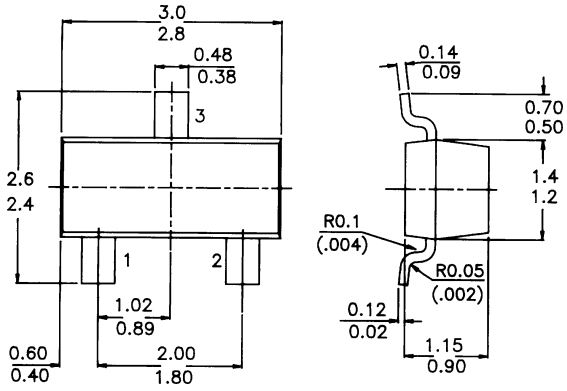
CSC2712Y=1E
CSC2712GR(G)=1F
CSC2712BL(L)=1G

Pin configuration

1 = BASE
2 = EMITTER
3 = COLLECTOR



PACKAGE OUTLINE DETAILS
ALL DIMENSIONS IN mm



ABSOLUTE MAXIMUM RATINGS

Collector-base voltage (open emitter)	V_{CBO}	*max.*	*60 V*
Collector-emitter voltage (open base)	V_{CEO}	*max.*	*50 V*
Emitter-base voltage (open collector)	V_{EBO}	*max.*	*5 V*
Collector current (peak value)	I_C	*max.*	*150 mA*
Total power dissipation at T_{amb} = 25°C	P_{tot}	*max.*	*150 mW*
Junction temperature	T_j	*max.*	*150 ° C*
D.C. current gain			
$-I_C$ = 2 mA; $-V_{CE}$ = 6V	h_{FE}	*min.*	*70*
		max.	*700*
Transition frequency			
I_C = 1 mA; V_{CE} = 10 V	f_T	*min.*	*80 MHz*
Noise figure at R_S = 10 KW			
I_C = 0.1 mA; V_{CE} = 6V;			
f = 1 kHz	*F*	*max*	*10 dB*

RATINGS *(at T_A = 25°C unless otherwise specified)*

Limiting values			
Collector-base voltage (open emitter)	V_{CBO}	*max.*	*60 V*
Collector-emitter voltage (open base)	V_{CEO}	*max.*	*50 V*
Emitter-base voltage (open collector)	V_{EBO}	*max.*	*5 V*
Collector current (d.c.)	I_C	*max.*	*150 mA*
Base current	I_B	*max.*	*30 mA*
Total power dissipation at T_{amb} = 25°C	P_{tot}	*max.*	*150 mW*
Junction temperature	T_j	*max.*	*150 °C*
Storage temperature	*Tstg*	*–50 to*	*+150 °C*

CHARACTERISTICS *(at T_A = 25°C unless otherwise specified)*

Collector cut-off current			
I_E = 0; V_{CB} = 60 V	I_{CBO}	*max.*	*100 nA*
Emitter cut-off current			
I_C = 0; V_{EB} = 5 V	I_{EBO}	*max.*	*100 nA*
Saturation voltage			
I_C = 100 mA; I_B = 10 mA	V_{CEsat}	*max.*	*250 mV*
D.C. current gain			
I_C = 2 mA; V_{CE} = 6 V	h_{FE}	*min.*	*70*
		max.	*700*
	Y	*min.*	*120*
		max.	*240*
	GR(G)	*min.*	*200*
		max.	*400*
	BL(L)	*min.*	*350*
		max.	*700*
Transition frequency			
I_C = 1 mA; V_{CE} = 10 V	f_T	*min.*	*80 MHz*
Noise figure at R_g = 10 kW			
V_{CE} = 6 V; I_C = 0.1 mA			
f = 1 kHz	N_F	*max.*	*10 dB*

Notes

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished on the CDIL Web Site/ CD is believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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